

Fig 1A

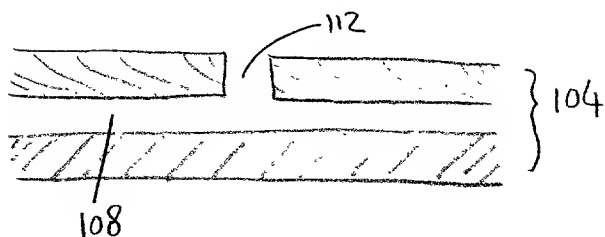


Fig 1B

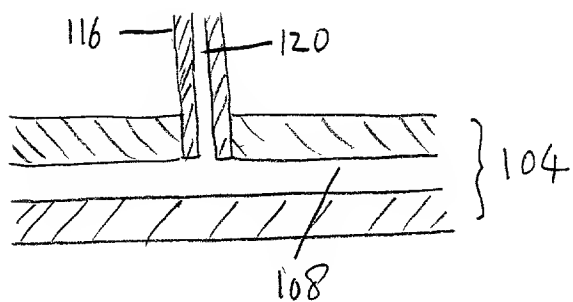


Fig 1C

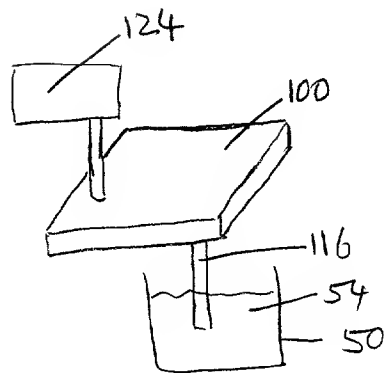


Fig 2A

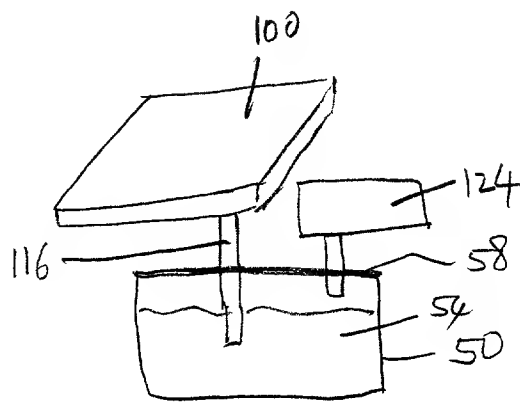


Fig 2B

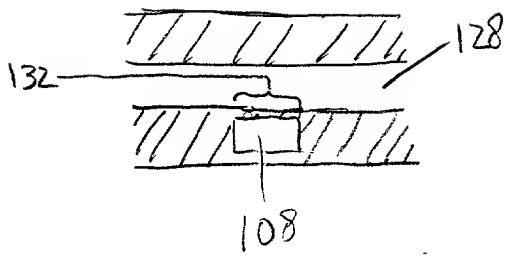


Fig 3A

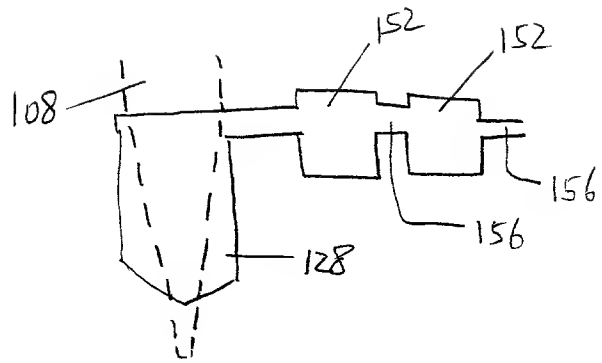


Fig 3B

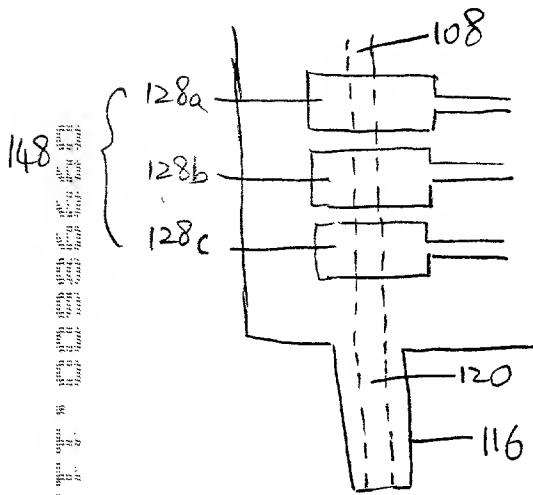


Fig 3C

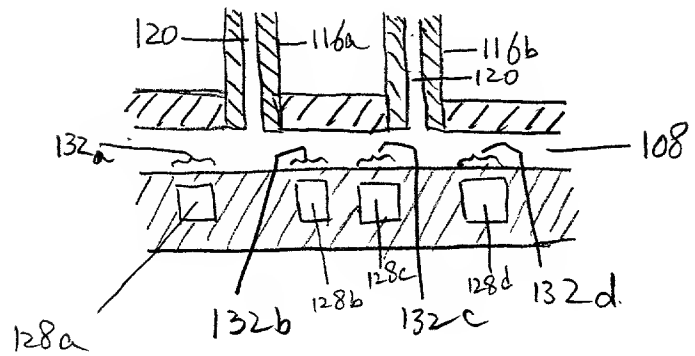


Fig 3D

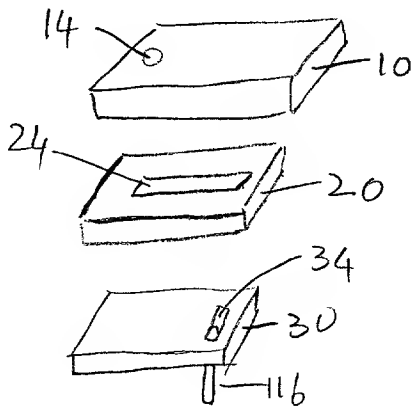
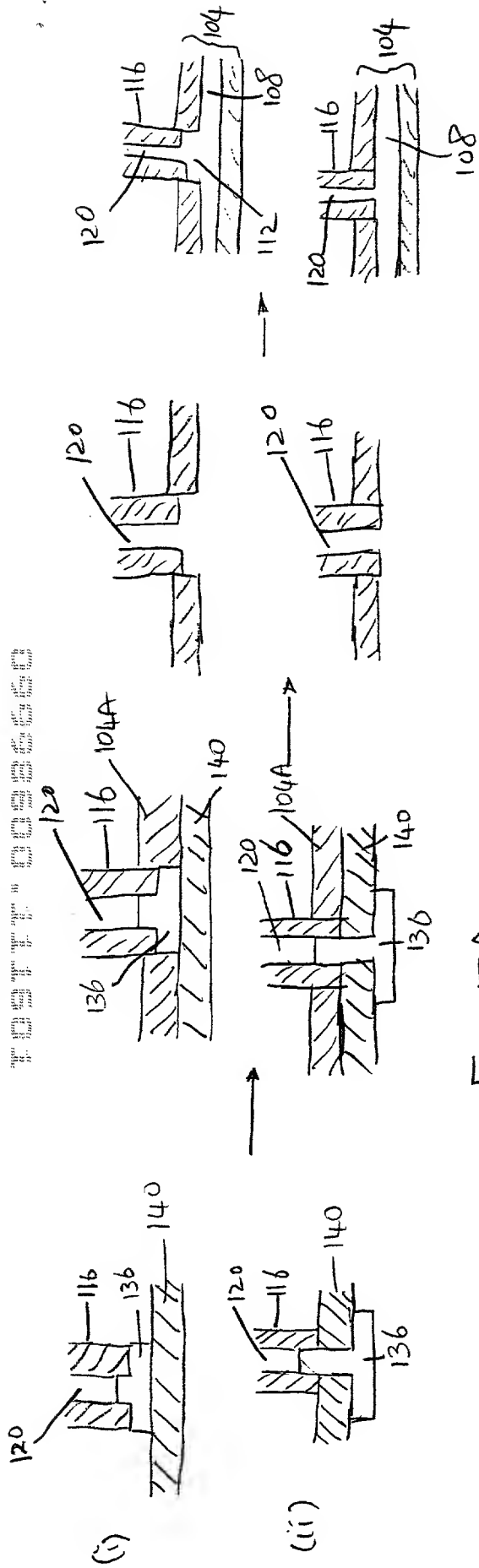
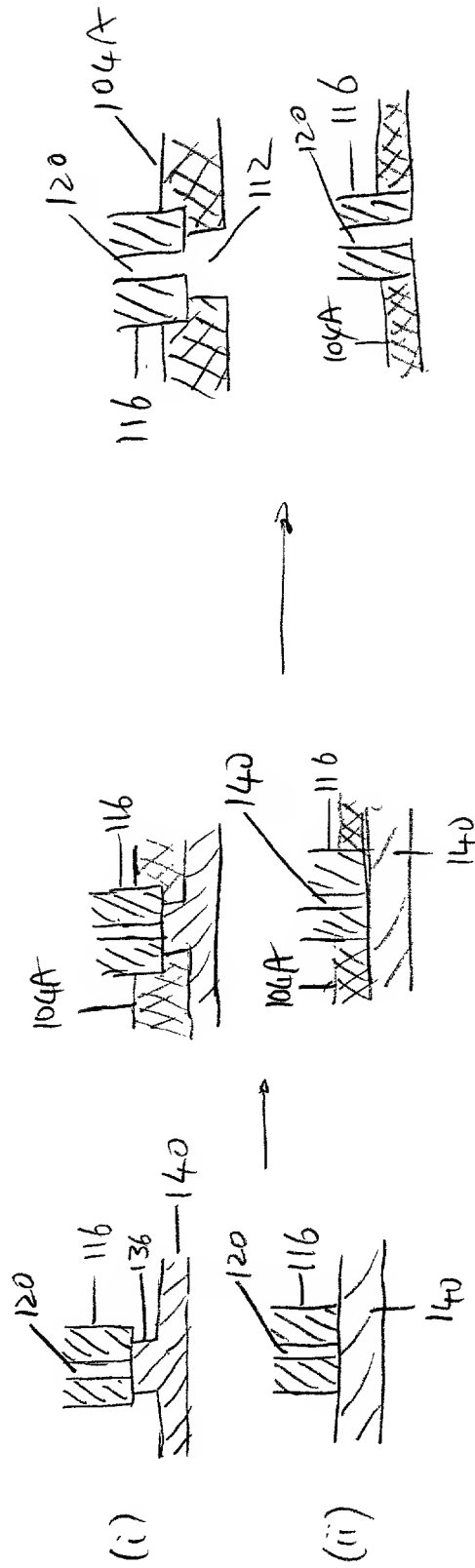


Fig 4


$$\begin{array}{c} \Delta \\ 5 \\ \hline 49 \end{array}$$


557

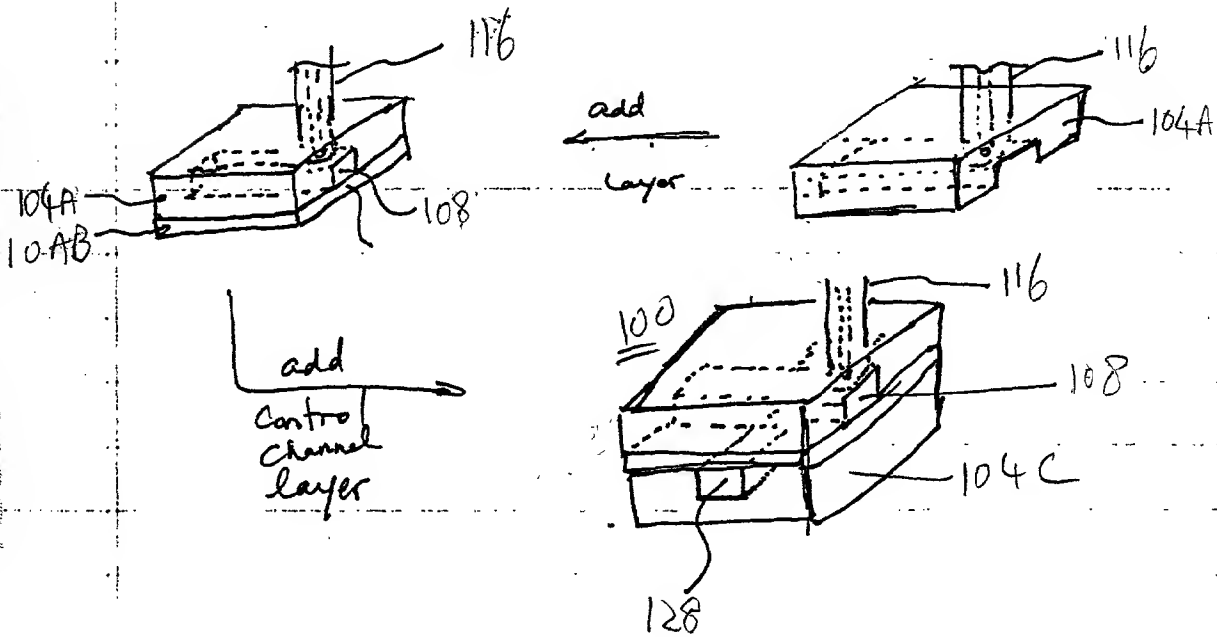
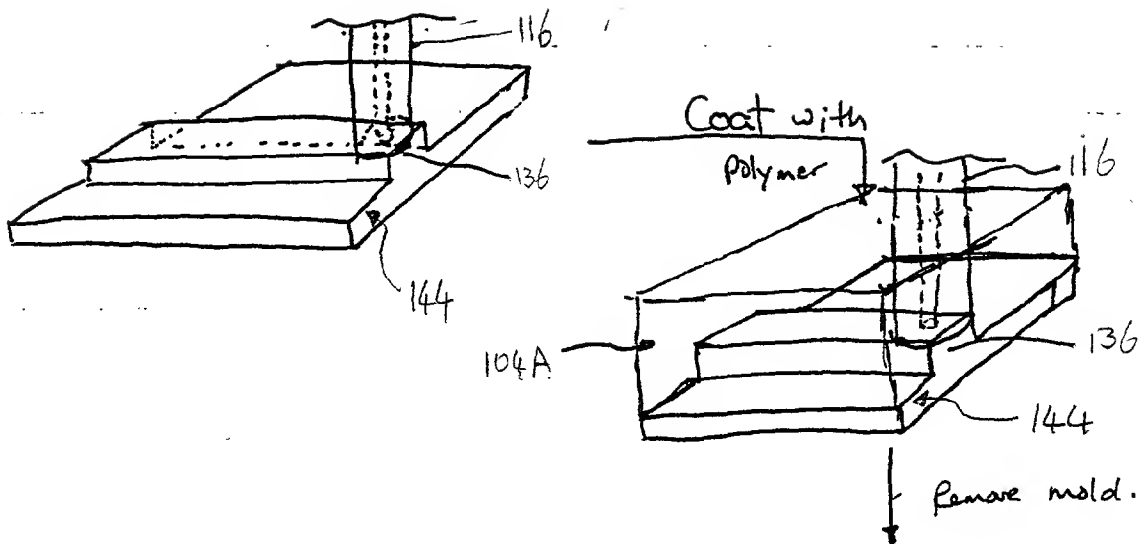


Figure 5C

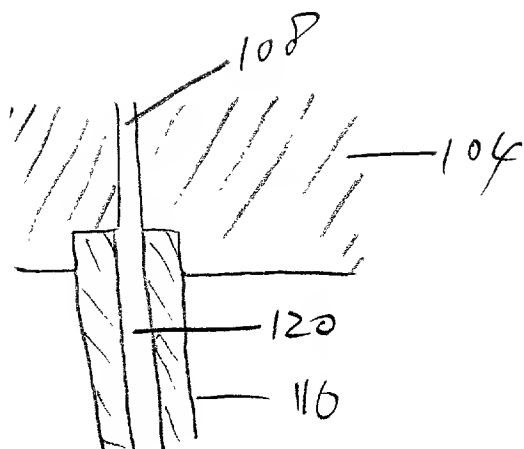
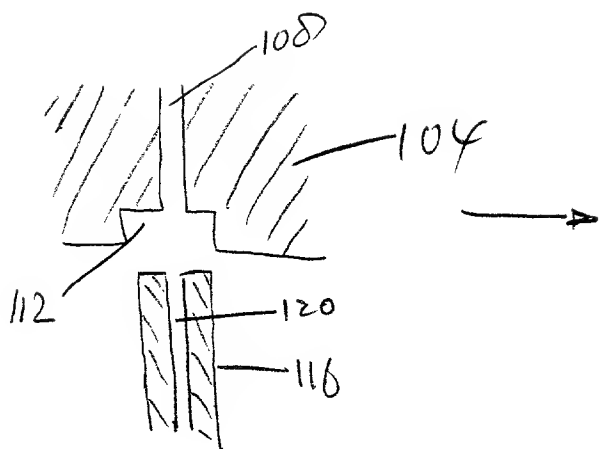


Fig 6A

112
 108
 104
 120
 116

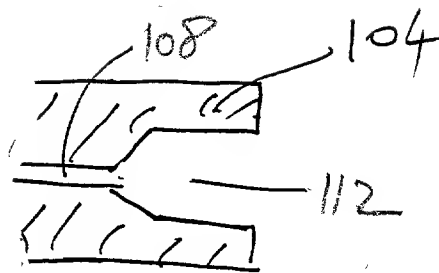
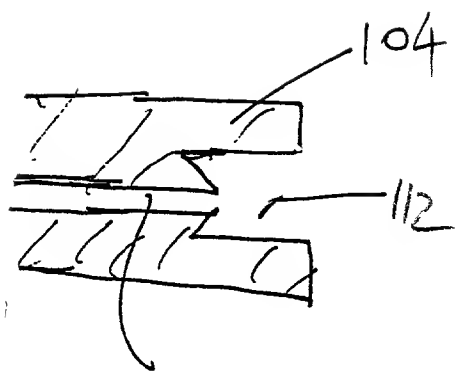


Fig 6B

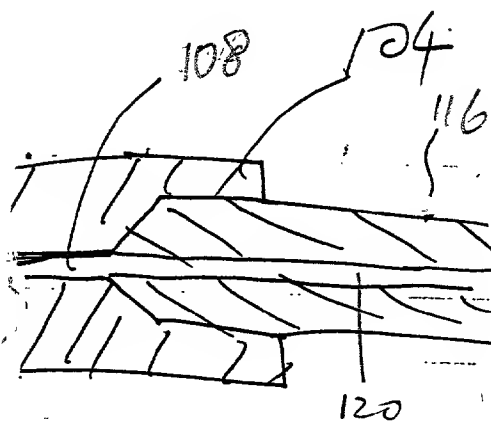
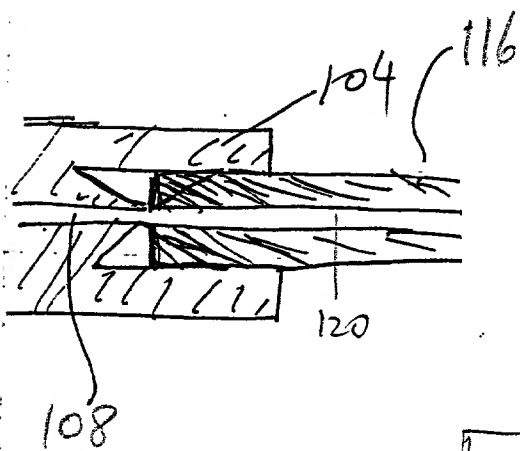


Fig 6C

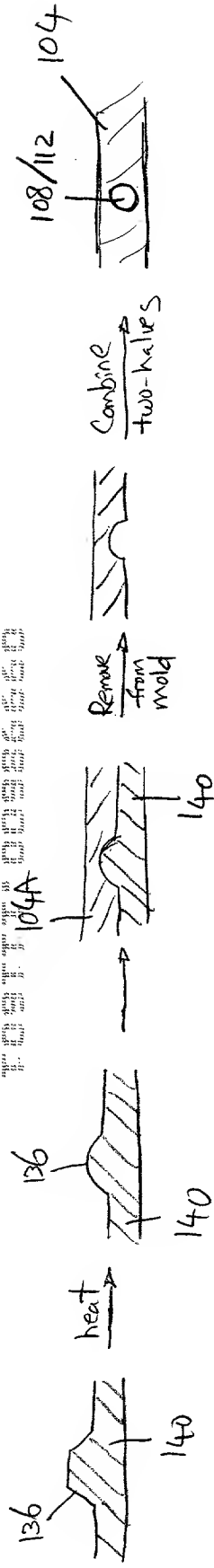
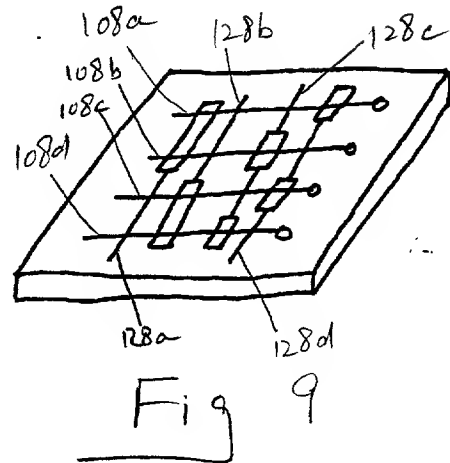
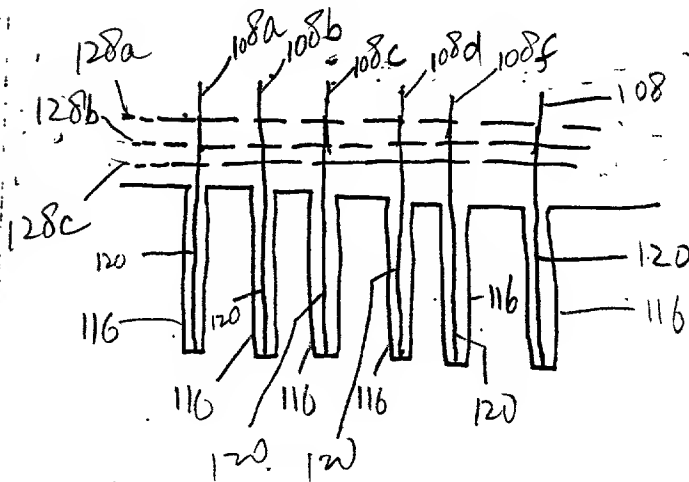
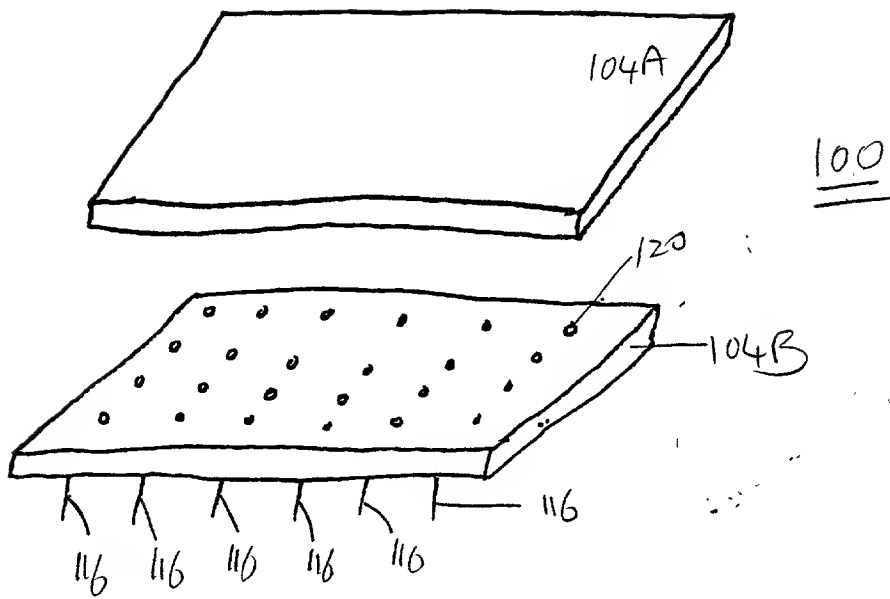


Fig 7



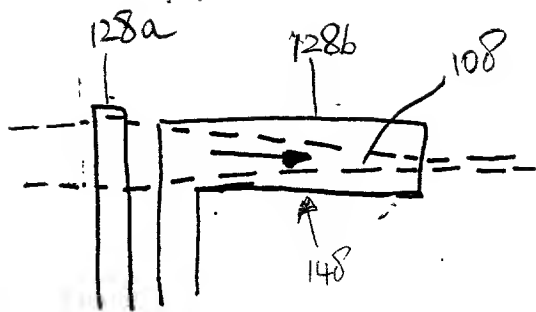


Fig 10A

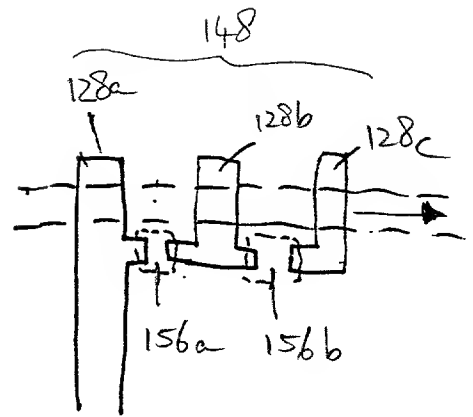


Fig 10E

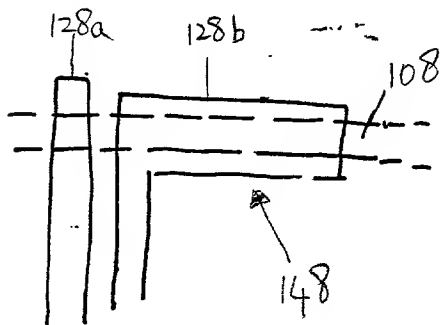


Fig 10B

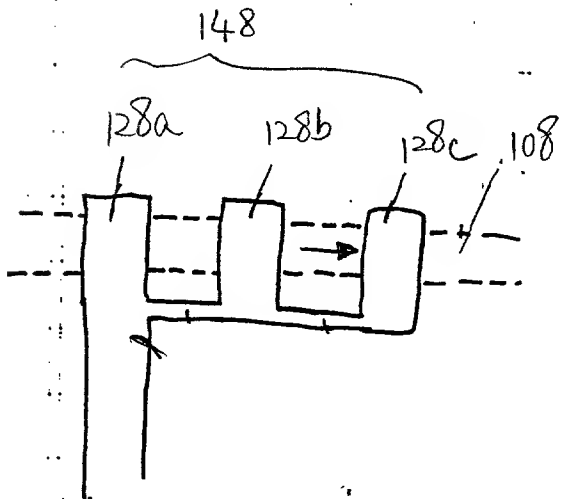


Fig 10C

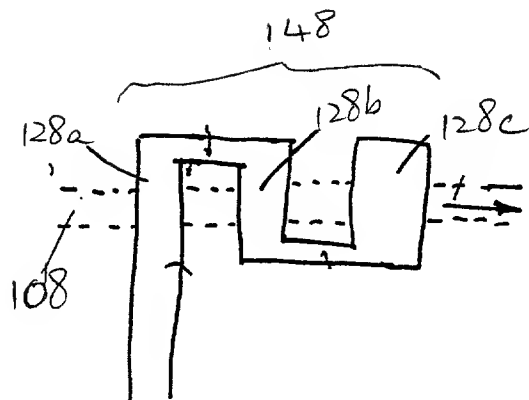


Fig 10D

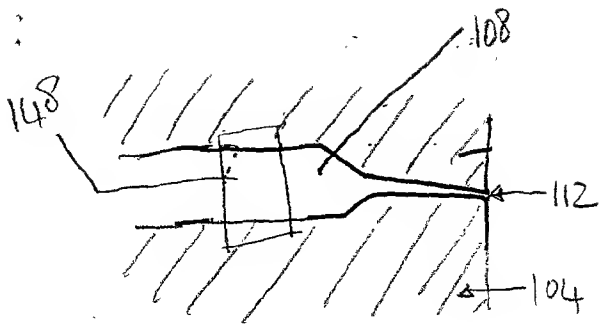


Fig 11B

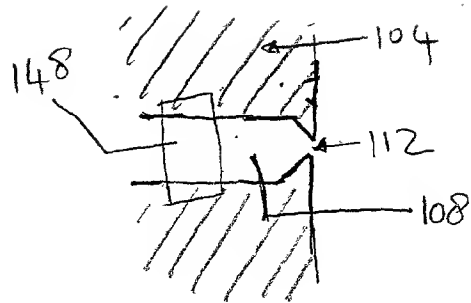


Fig 11C

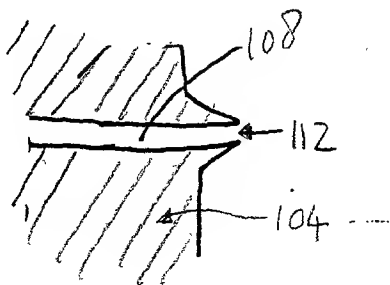


Fig 11A

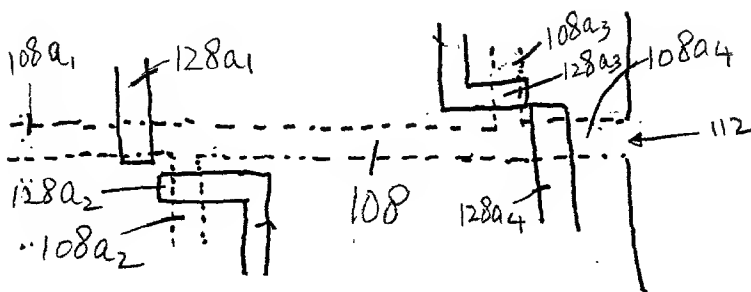


Fig 12A

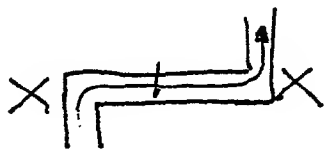


Fig 12B

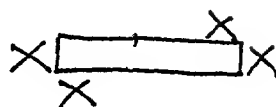


Fig 12C

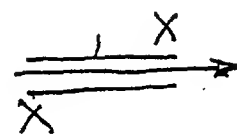
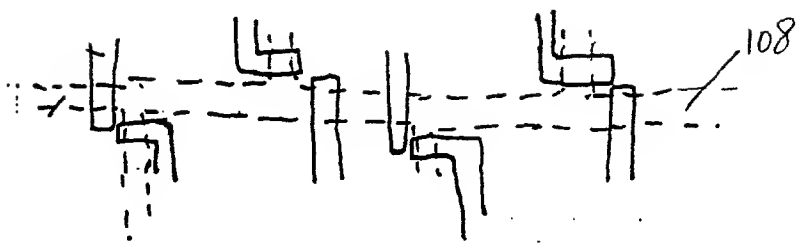


Fig 12D



12E

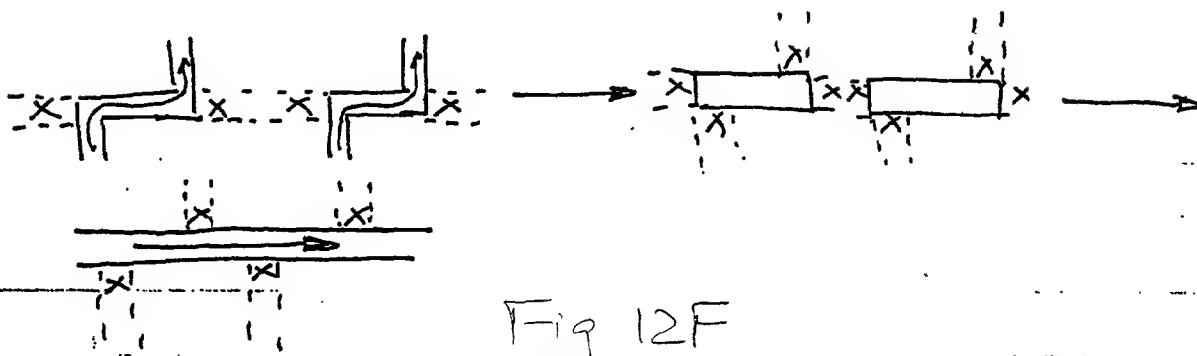


Fig 12F

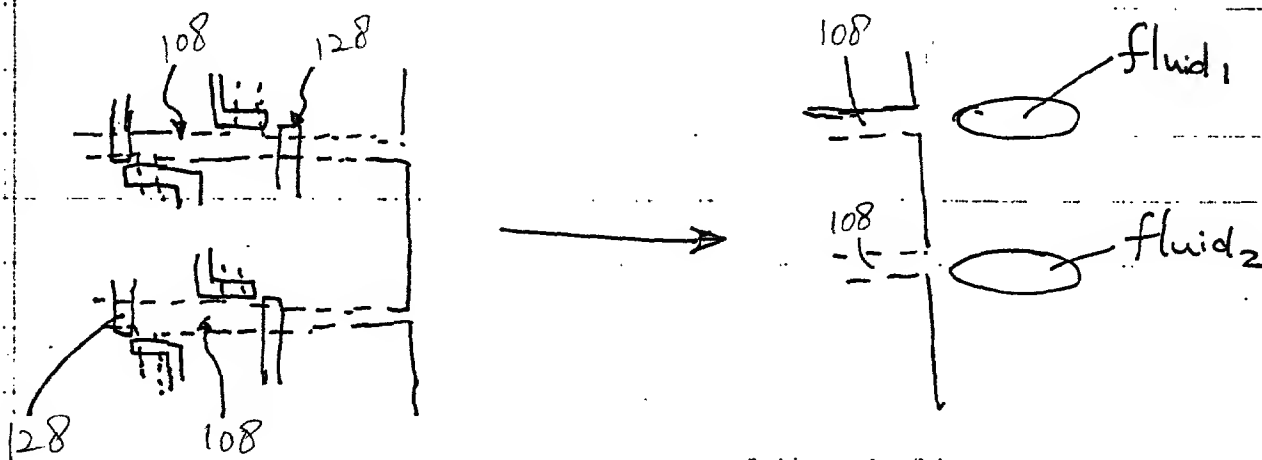


Fig 12G

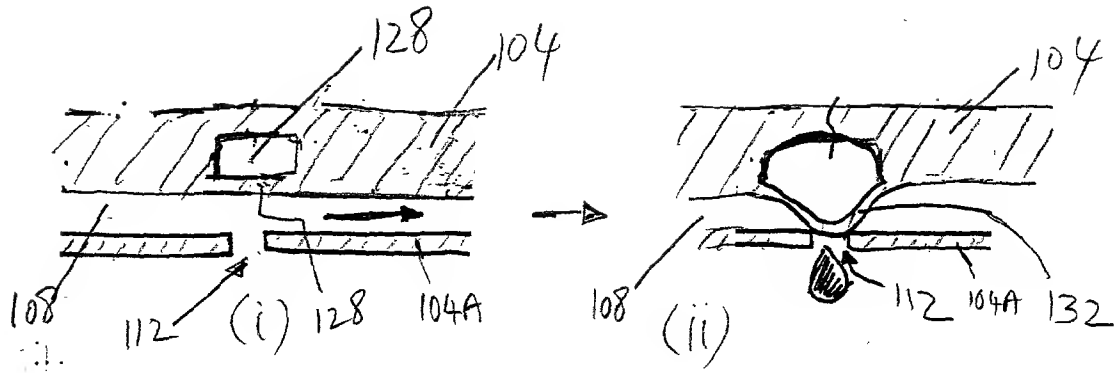


Fig 13A

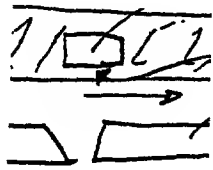


Fig 13B

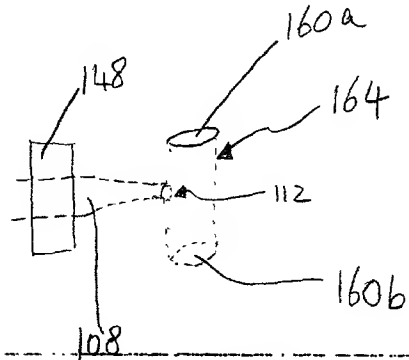


Fig 15A

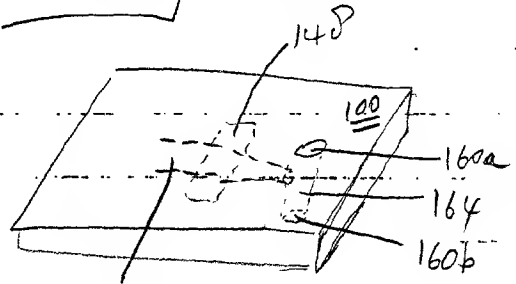


Fig 15B

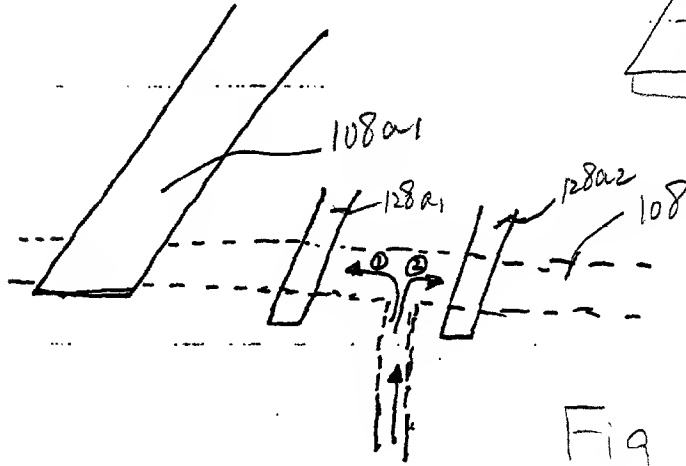


Fig 14A

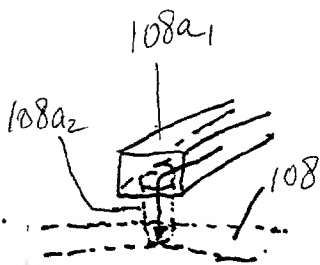


Fig 14B

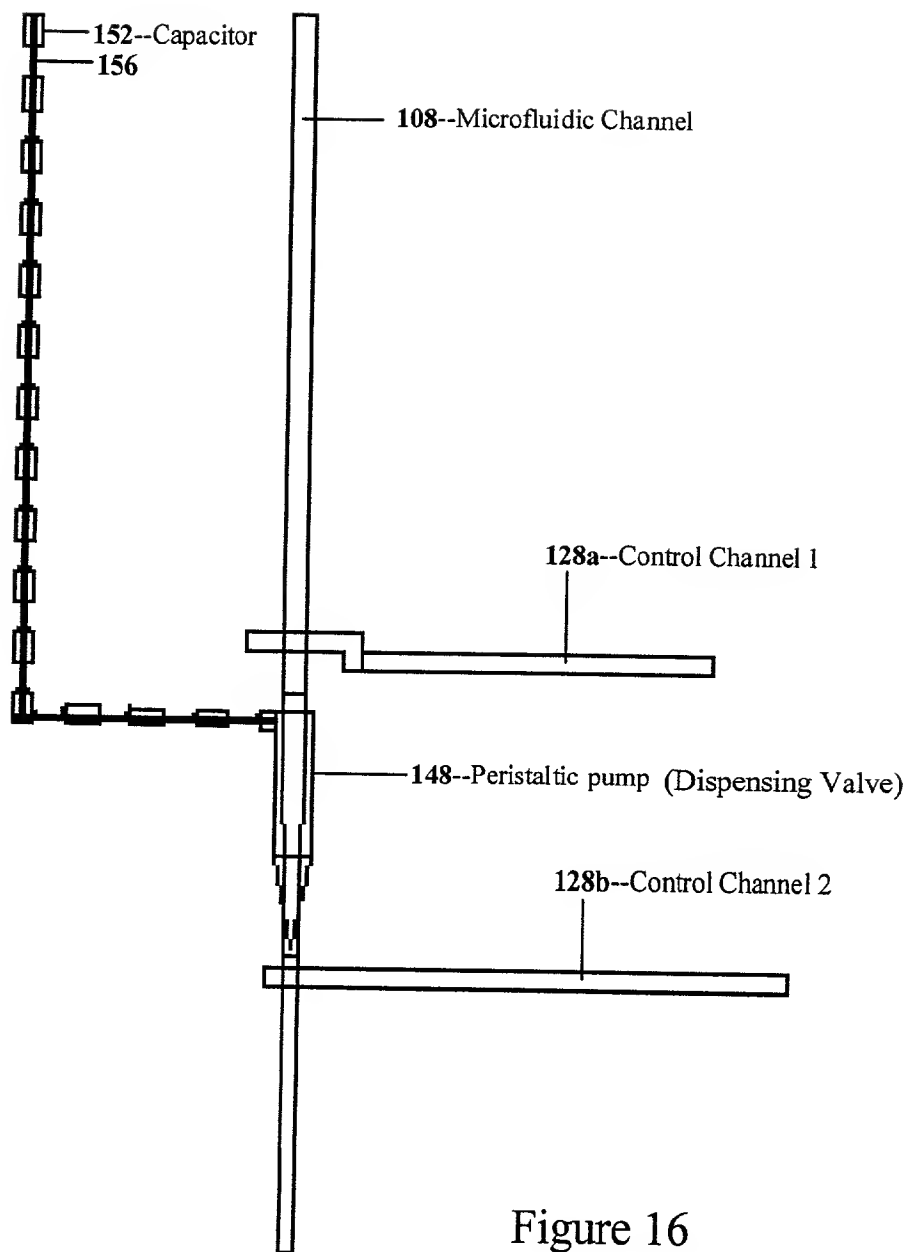


Figure 16

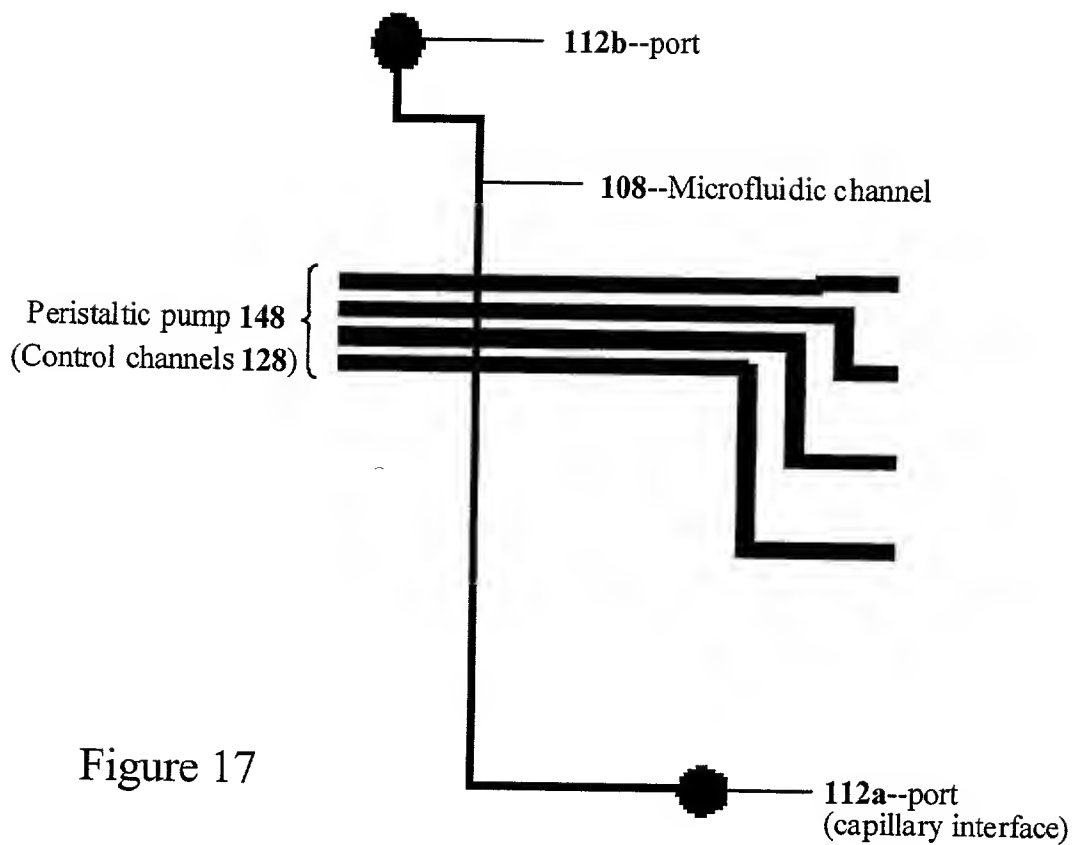


Figure 17

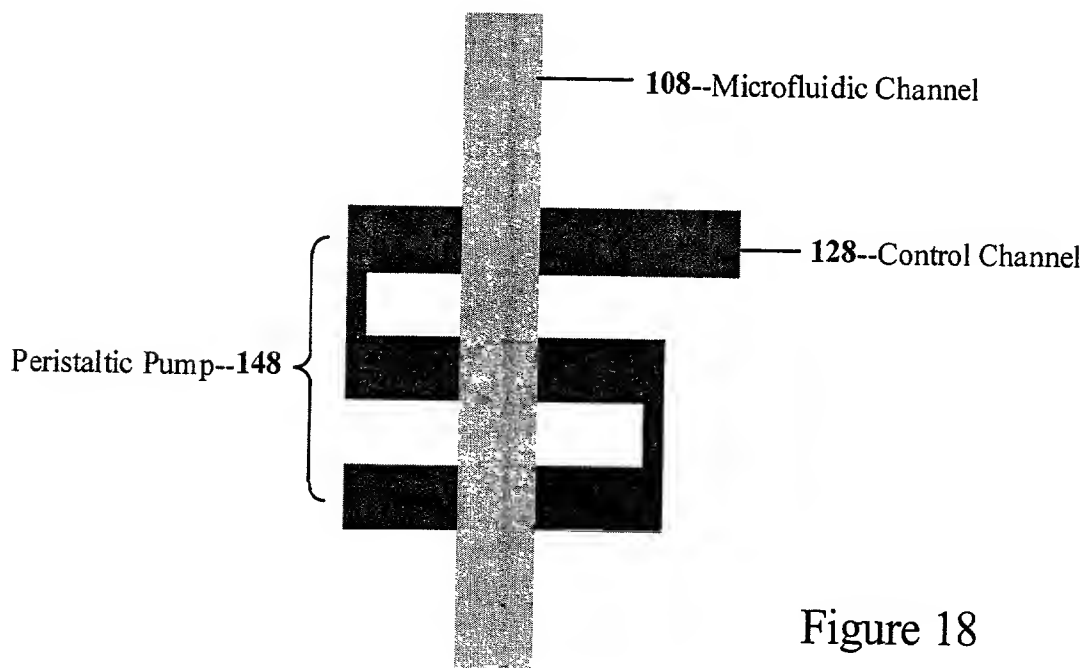


Figure 18

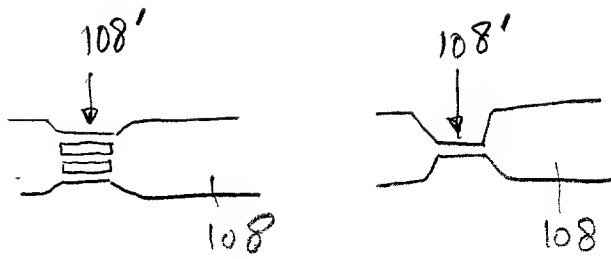


Fig 19

FIG. 20A

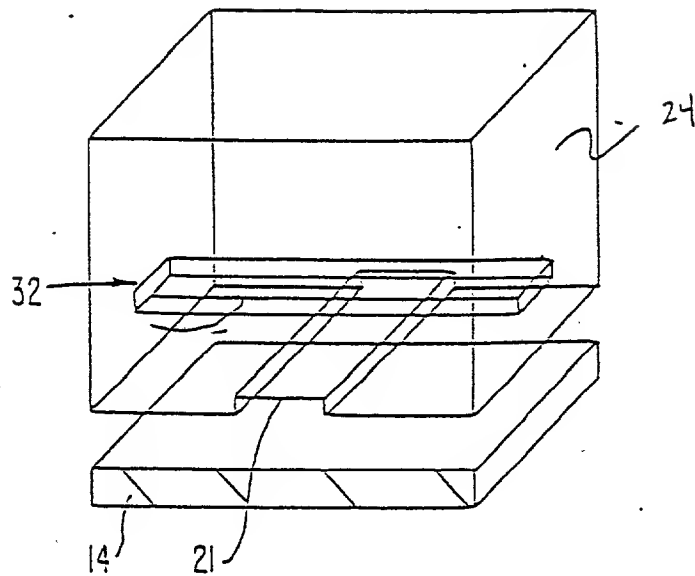
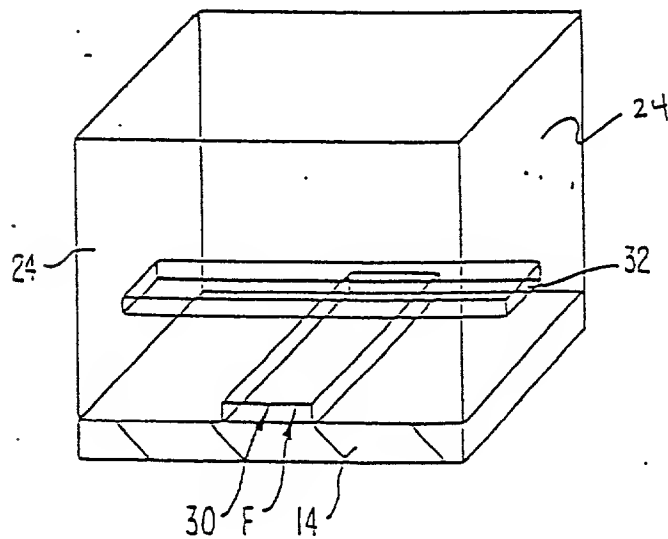


FIG. 20B



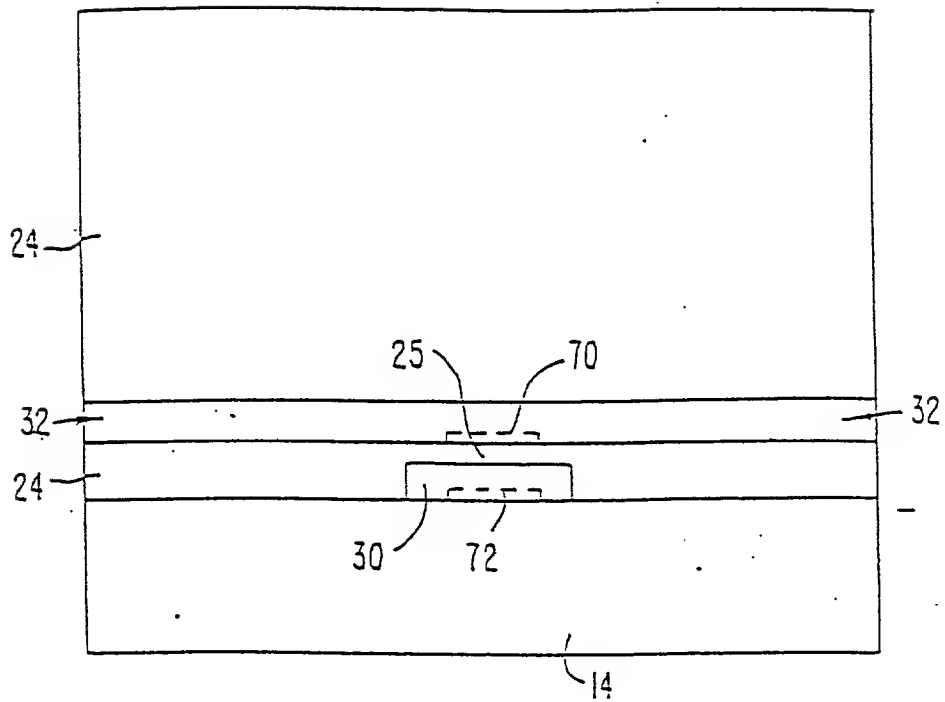


FIG. 21A

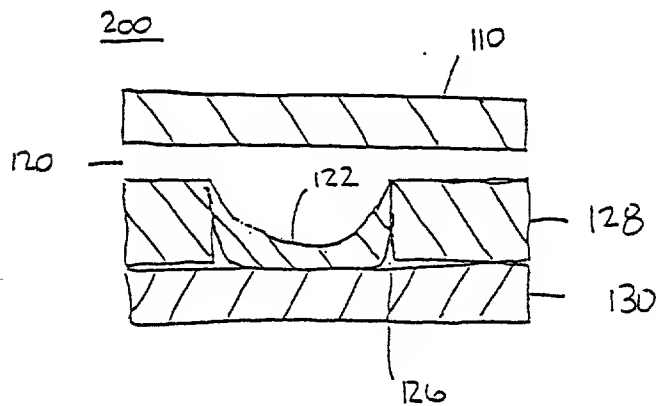


FIG. 21B

FIG. 22A is a cross-sectional view of a device 4800 in a first state. The device 4800 includes a substrate 4802 and a layer 4804. A layer 4806 is disposed on the substrate 4802, and a layer 4808 is disposed on the layer 4806. The layer 4808 is in contact with the layer 4804. The layer 4808 is a conductive layer, and the layer 4804 is an insulating layer. The layer 4806 is a conductive layer, and the layer 4802 is an insulating layer. The device 4800 is a semiconductor device, and the layer 4808 is a gate electrode. The layer 4804 is a gate dielectric, and the layer 4806 is a gate contact. The layer 4802 is a substrate, and the layer 4808 is a gate electrode. The device 4800 is a semiconductor device, and the layer 4808 is a gate electrode. The layer 4804 is a gate dielectric, and the layer 4806 is a gate contact. The layer 4802 is a substrate, and the layer 4808 is a gate electrode.

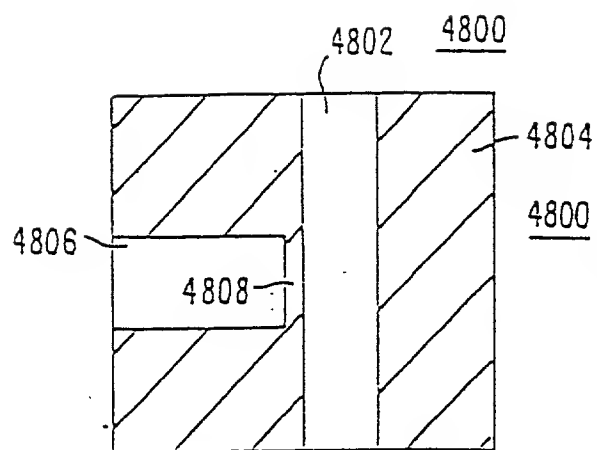


Fig 22A

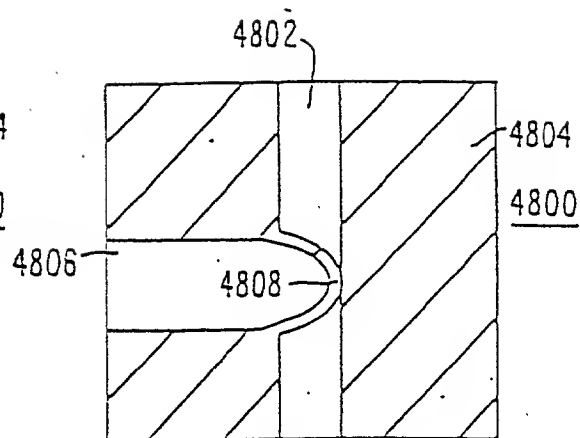


Fig 22B

Fig 23A

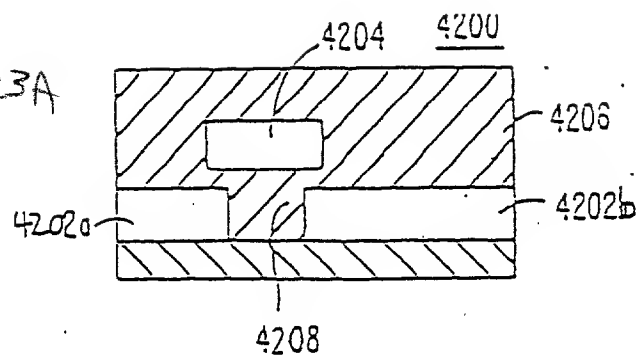
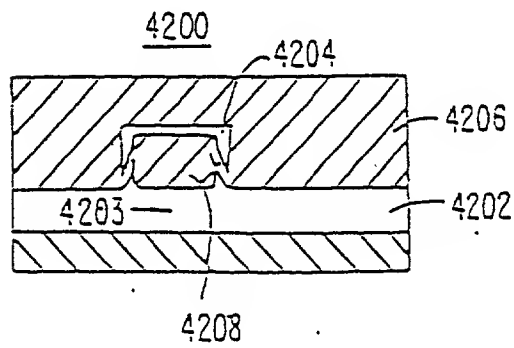


Fig 23B



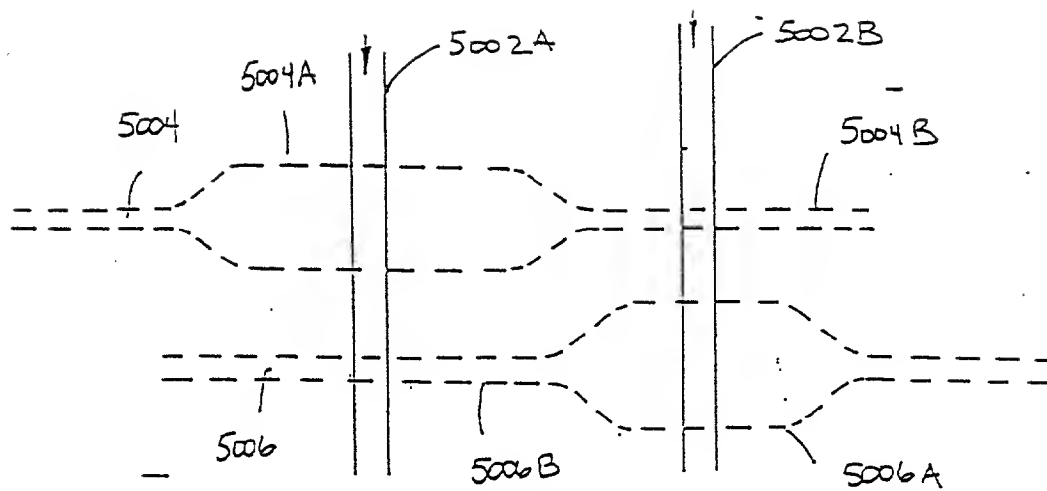


Fig 24

